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TR-935

DESIGN CRITERIA FOR STABILIZATION OF TRANSISTOR GAIN WITH TEMPERATURE

George N. Kambouris

15 May 1961

DIAMOND ORDNANCE FUZE LABORATORIES
ORDNANCE CORPS ● DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C.

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CONTENTS

ABSTRACT

An equation has been developed for a generalized transistor amplifier network, expressing the relationship that must be maintained between circuit elements and the transistor small-signal parameters for minimum gain variations over wide temperature ranges. Employing a single-stage common-emitter amplifier with collector-to-base feedback and various degrees of mismatch relative to the design criteria, the relationship was checked from -50 to +90° C at 10, 100, and 500 kc. Results show that considerable improvement in gain stability can be obtained in going from the unmatched to matched condition, but with some reduction in the overall gain, the loss being dependent on the relative magnitude of the generator and transistor input impedances.

The normalized gain variations were reduced from a maximum of 18 db to less than 2 db over the temperature range.

1. INTRODUCTION

One of the more perplexing problems arising with the use of transistors as active elements in amplifier circuits is that of gain variations with temperature.

Although many theoretical studies have been made and equations developed by various investigators (ref 1, 2) that indicate the temperature dependence of the intrinsic parameters of a transistor and under what conditions improvements could be expected, this temperature dependence is inherent in the materials, physics, and design of the device and cannot be readily corrected without degrading other performance characteristics. Although considerable improvement in the gain stability of transistor amplifiers is obtained with various temperature-compensating techniques (ref 3-5) and devices (such as thermistors, temperature-sensitive diodes, and degenerative feedback), the need for additional improvement still exists. Hence, the recent work by Schmeltzer (ref 6), showing that additional gain stability can be obtained when a given relationship is maintained between circuit elements and the temperature-dependence small-signal parameters of the transistor, is of considerable interest. His work, unfortunately, was limited in scope to a common-emitter amplifier circuit using an emitter resistance as the degenerative feedback.

The present investigation was initiated to develop a more generalized design equation expressing the relationship that should be maintained between circuit elements and transistor parameters for minimum gain variations over wide temperature ranges and that would be valid for any network configuration.

2. DEVELOPMENT

A general single-stage amplifier network can be represented by the circuit shown in figure 1 where the matrix [z] represents the active device in an unspecified configuration. From this general network, any

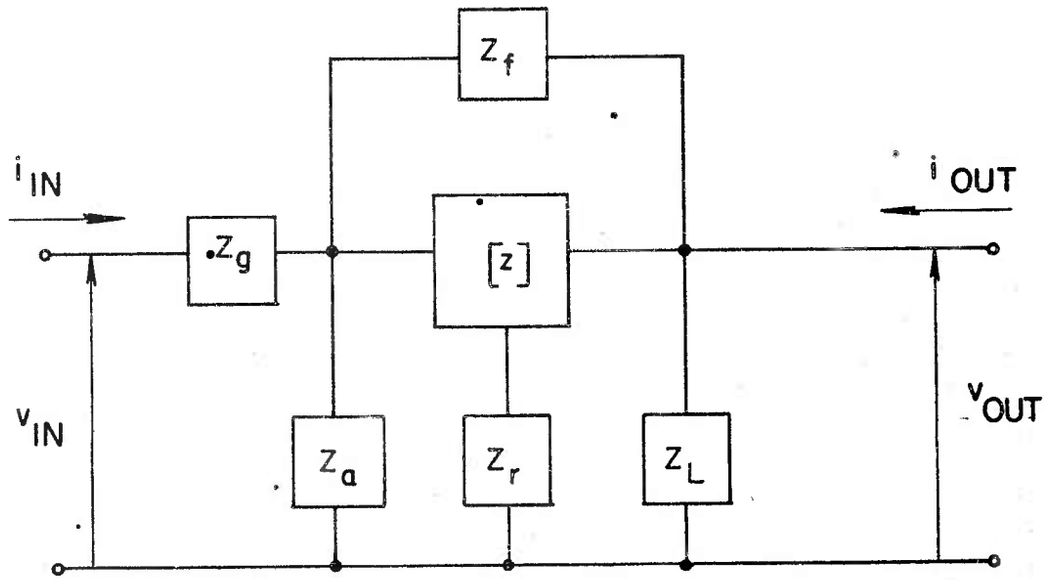


Figure 1. A generalized single-stage amplifier network.

specific amplifier circuit desired can be readily obtained by allowing the components Z_a, Z_f, Z_g, Z_r, Z_L to assume values from zero to infinity and the characteristic matrix [z] to describe the transistor configuration of interest.

To simplify the development of the overall voltage gain (A_v), the variation of which is to be minimized with respect to temperature changes, the general network in figure 1 is subdivided into four subnetworks as indicated in figure 2. From the equations relating the currents and voltages of the subnetworks, the terminal characteristics of each can be obtained and, if properly combined, the overall terminal characteristics and voltage gain equation of the general network derived.

2.1 Terminal Characteristics

Starting with the individual subnetworks (A,B,C, and D), the characteristic equations describing the terminal behavior are:

Subnetwork A

$$i_1 = i_2 \tag{1}$$

$$v_1 = v_2 + Z_g\, i_2 \tag{2}$$

or in matrix form

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A_A \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{3}$$

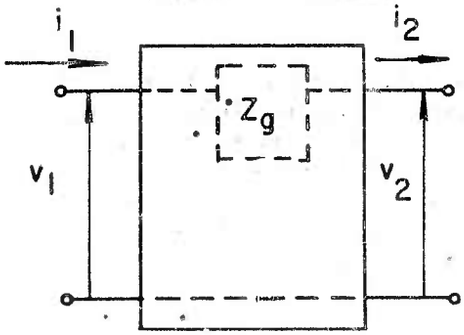
where

$$\begin{bmatrix} A_A \end{bmatrix} = \begin{bmatrix} (1) & (+Z_g) \\ (0) & (1) \end{bmatrix} \tag{4}$$

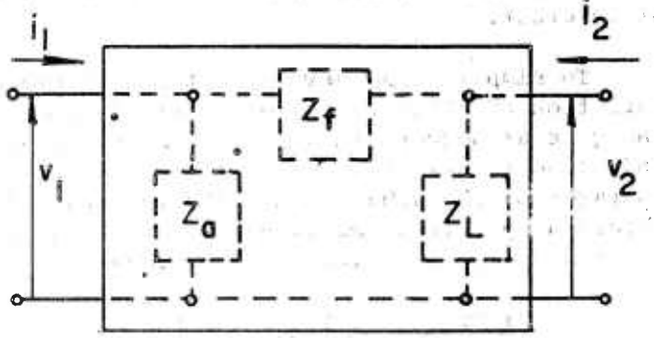
Subnetwork B

$$i_1 = (Y_a + Y_f)\, v_1 - Y_f v_2 \tag{5}$$

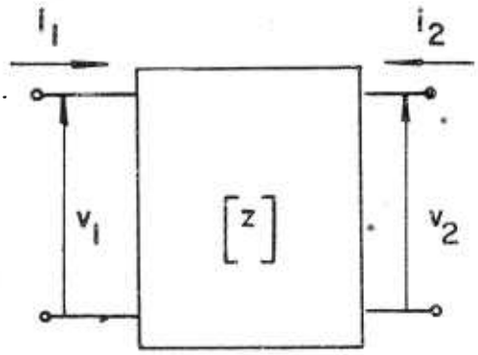
$$i_2 = -Y_f v_1 + (Y_L + Y_f)\, v_2 \tag{6}$$



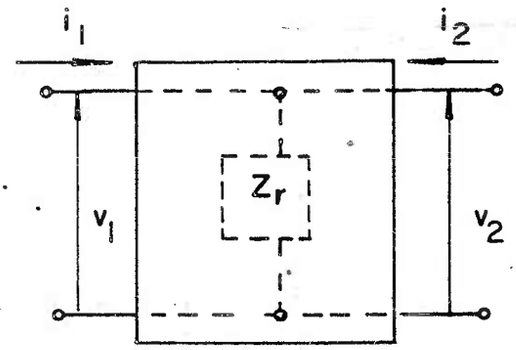
a. Subnetwork A



b. Subnetwork B



c. Subnetwork C



d. Subnetwork D

Figure 2. Subnetworks of the general network.

in matrix form

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_B \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{7}$$

where

$$\begin{bmatrix} Y_B \end{bmatrix} = \begin{bmatrix} (Y_a + Y_f) & (-Y_f) \\ (-Y_f) & (Y_L + Y_f) \end{bmatrix} \tag{8}$$

Subnetwork C

$$v_1 = z_{11}i_1 + z_{12}i_2 \tag{9}$$

$$v_2 = z_{21}i_1 + z_{22}i_2 \tag{10}$$

in matrix form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = [z] \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{11}$$

where

$$[z] = \begin{bmatrix} (z_{11}) & (z_{12}) \\ (z_{21}) & (z_{22}) \end{bmatrix} \tag{12}$$

Subnetwork D

$$v_1 = v_2 \tag{13}$$

$$v_2 = Z_r i_1 + Z_r i_2 \tag{14}$$

in matrix form

$$\begin{bmatrix} v_i \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_D \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{15}$$

where

$$\left[Z_D\right] = \begin{bmatrix} (Z_r) & (Z_r) \\ (Z_r) & (Z_r) \end{bmatrix} \tag{16}$$

The subnetworks are now combined as shown in figure 3.

Beginning with the series combination shown in figure 3a it is apparent that

$$v_1 = v_1' + v_1'' \tag{17}$$

$$v_2 = v_2' + v_2'' \tag{18}$$

$$i_1 = i_1' = i_1'' \tag{19}$$

$$i_2 = i_2'' = i_2'' \tag{20}$$

and if the indicated operations of equations (17) and (18) are complied with, the characteristic equations of subnetwork CD are obtained and can be expressed as

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \left[Z_{CD}\right] \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{21}$$

where

$$\left[Z_{CD}\right] = \begin{bmatrix} (z_{11} + Z_r) & (z_{12} + Z_r) \\ (z_{21} + Z_r) & (z_{22} + Z_r) \end{bmatrix} \tag{22}$$

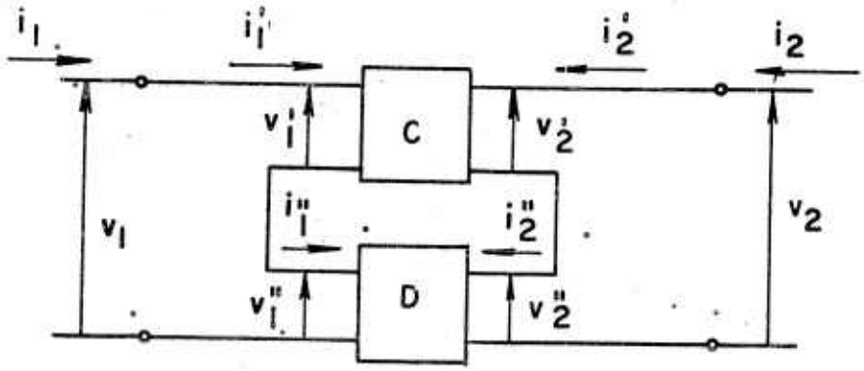
Next, with the parallel combination of subnetworks B and CD (fig 3b), the following relationships exist.

$$i_1 = i_1' + i_1'' \tag{23}$$

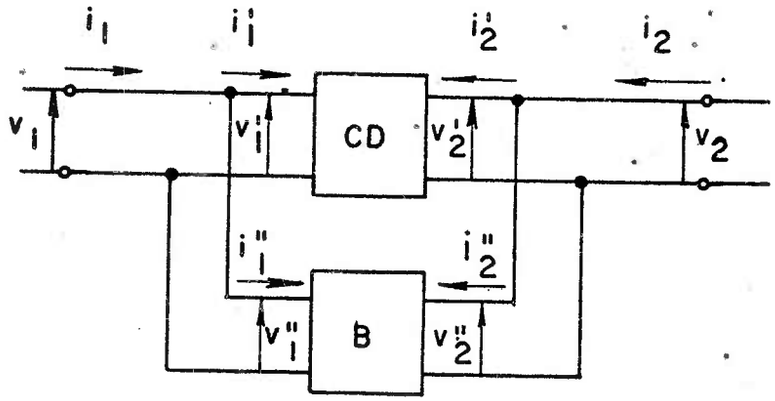
$$i_2 = i_2' + i_2'' \tag{24}$$

$$v_1 = v_1' = v_1'' \tag{25}$$

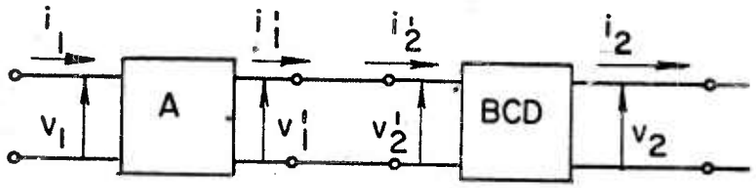
$$v_2 = v_2' = v_2'' \tag{26}$$



a. Series combination of subnetworks C and D.



b. Parallel combination of subnetworks B and CD.



c. Cascade combination of subnetworks A and BCD.

Figure 3. Combination of subnetworks to form the generalized network.

From the operations indicated by equations (23) and (24), the terminal equations for subnetwork BCD are

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{BCD} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{27}$$

where

$$\begin{bmatrix} Y_{BCD} \end{bmatrix} = \begin{bmatrix} (Y_a + Y_f + \dfrac{z_{22} + Z_r}{\Delta z + Z_r z_s}) & (-Y_f - \dfrac{z_{12} + Z_r}{\Delta z + Z_r z_s}) \\ (-Y_f - \dfrac{z_{21} + Z_r}{\Delta z + Z_r z_s}) & (Y_L + Y_f + \dfrac{z_{11} + Z_r}{\Delta z + Z_r z_s}) \end{bmatrix} \tag{28}$$

and

$$\Delta z = z_{11} z_{22} - z_{12} z_{21} \tag{29}$$

$$z_s = z_{11} + z_{22} - z_{12} - z_{21} \tag{30}$$

Finally, subnetworks A and BCD are now cascaded as shown in figure 3c where the characteristic equation for each subnetwork is expressed as

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A_A \end{bmatrix} \begin{bmatrix} v_1' \\ i_1' \end{bmatrix} \tag{31}$$

for subnetwork A, and

$$\begin{bmatrix} v_2' \\ i_2' \end{bmatrix} = \begin{bmatrix} A_{BCD} \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{32}$$

for subnetwork BCD. However, since

$$v_1' = v_2' \tag{33}$$

and

$$i_1' = i_2' \tag{34}$$

then

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A_A \end{bmatrix} \begin{bmatrix} v_1' \\ i_1' \end{bmatrix} = \begin{bmatrix} A_A \end{bmatrix} \begin{bmatrix} v_2' \\ i_2' \end{bmatrix} = \begin{bmatrix} A_A \end{bmatrix} \begin{bmatrix} A_{BCD} \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{35}$$

or

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{36}$$

By proper transformation, equation (36) can be rewritten and expressed in the form

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{37}$$

where the elements of Z are the terminal characteristic impedances of the generalized network:

$$Z_{11} = Z_g + \frac{z_{11}+Z_r+(Y_L+Y_f)\ (\Delta z+Z_r z_s}{K+K_1 z_s + Y_s\ \Delta z+Y_a z_{11}+Y_L z_{22}} \tag{38}$$

$$Z_{12} = \frac{z_{12}+Z_r + Y_f(\Delta z+Z_r z_s)}{K+K_1 z_s + Y_s\ \Delta z+Y_a z_{11}+Y_L z_{22}} \tag{39}$$

$$Z_{21} = \frac{z_{21}+Z_r + Y_f(\Delta z+Z_r z_s)}{K+K_1 z_s + Y_s\ \Delta z + Y_a z_{11}+Y_L z_{22}} \tag{40}$$

$$Z_{22} = \frac{z_{22}+Z_r + (Y_a+Y_f)\ (\Delta z+Z_r z_s}{K+K_1 z_s + Y_s\ \Delta z + Y_a z_{11}+Y_L z_{22}} \tag{41}$$

and

$$K = 1 + Z_r\ (Y_a+Y_L) \tag{42}$$

$$K_i = Y_s Z_r + Y_f \tag{43}$$

$$Y_s = Y_a Y_L + Y_a Y_f + Y_f Y_L \tag{44}$$

$$z_s = z_{11} + z_{22} - z_{12} - z_{21} \tag{45}$$

$$\Delta z = z_{11} z_{22} - z_{12} z_{21}. \tag{46}$$

2.2 Voltage Gain

With the voltage gain of any system defined

$$A_v = \frac{v_{out}}{v_{in}} \tag{47a}$$

the overall gain of the generalized network can be expressed as

$$A_v = \frac{Z_{21} i_1 + Z_{22} i_2}{Z_{11} i_1 + Z_{12} i_2} \tag{47b}$$

By assuming that $i_2 = 0$ (fig 1), the gain expression reduces to

$$A_v = \frac{Z_{21}}{Z_{11}} \tag{48}$$

Substituting into the above relation, equations (38) and (40), the overall voltage gain is obtained as a function of the general network and active device terminal parameters

$$A_v = \frac{Z_{21} + Z_r + Y_f (\Delta z + Z_r z_s)}{k + k_1 \Delta z + k_2 z_s + k_3 z_{11} + k_4 z_{22}} \tag{49}$$

where

$$k = Z_g Z_r (Y_g + Y_a + Y_L + Y_r) \tag{50}$$

$$k_1 = Z_g (Y_a Y_L + Y_a Y_f + Y_f Y_L) + Y_L + Y_f \tag{51}$$

$$k_2 = Z_g Z_r (Y_a Y_L + Y_a Y_f + Y_f Y_L) + Z_g Y_f + Z_r Y_L + Z_r Y_f \tag{52}$$

$$k_3 = Y_a Z_g + 1 \tag{53}$$

$$k_4 = Y_L Z_g \tag{54}$$

Finally, in order to express the gain in terms of temperature dependent transistor equivalent circuit parameters, it is necessary to substitute for the black-box a specific transistor equivalent circuit. With common-emitter orientations predominating in amplifier circuits, further development will be confined to the common-emitter hybrid-π equivalent circuit (ref 8) shown in figure 4. To simplify the development for the terminal characteristics, in terms of the equivalent circuit parameters, the hybrid-π representation is generalized to that in figure 4b where

$$Z_1 = r_{bb'} \tag{55}$$

$$Z_2 = r_{b'e} \,||\, C_{b'e} \tag{56}$$

$$Z_3 = r_{b'c} \,||\, C_{b'c} \tag{57}$$

$$Z_4 = r_{ce} \,||\, C_{ce} \tag{58}$$

Solving the loop equations

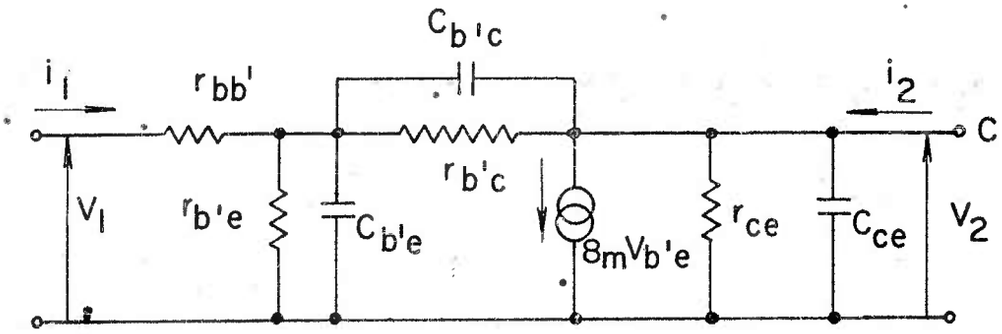
$$v_1 = (Z_1 + Z_2) i_1 + Z_2 i_3 \tag{59}$$

$$0 = (Z_2 + Z_3 + Z_4) i_3 + Z_2 i_1 - Z_4 i_2 + g_m r_{be} Z_4 \tag{60}$$

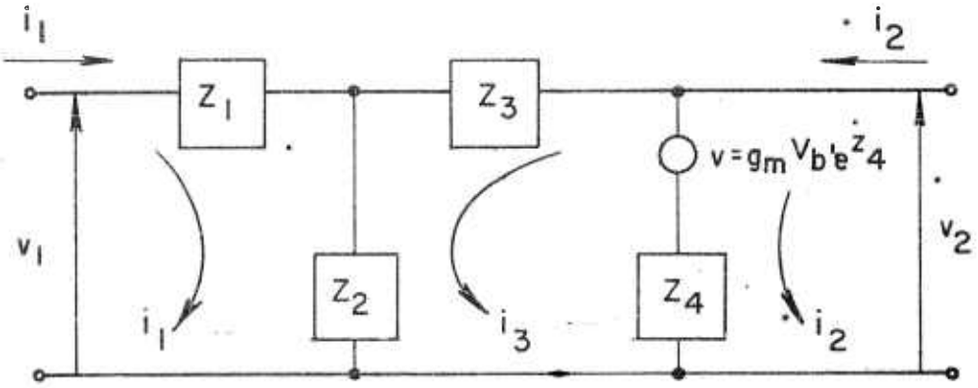
$$V_2 = Z_4 i_2 - g_m V_{b'e} Z_4 - Z_4 i_3 \tag{61}$$

for v_1 and v_2 as functions of i_1 and i_2 we get

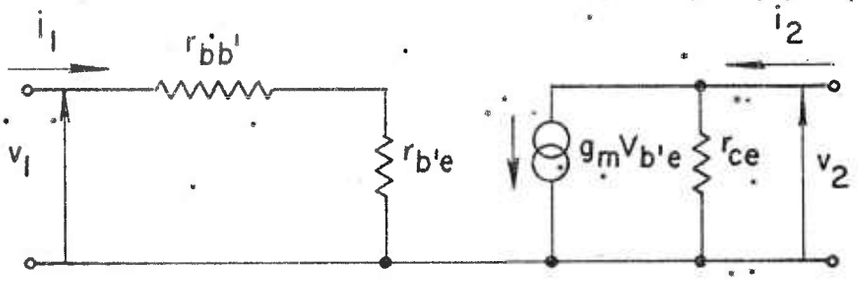
$$\begin{bmatrix} v_1 \\ \\ v_2 \end{bmatrix} = [z] \begin{bmatrix} i_1 \\ \\ i_2 \end{bmatrix} \tag{62}$$



a. Giacoletto hybrid-π equivalent circuit



b. Generalized hybrid-π network.



c. Simplified hybrid-π equivalent circuit for low frequencies.

Figure 4. Transistor equivalent circuits.

where

$$z_{11} = Z_1 + \frac{Z_2(Z_3+Z_4)}{Z_2+Z_3+Z_4+Z_2Z_4g_m} \tag{63}$$

$$z_{12} = \frac{Z_2Z_4}{Z_2+Z_3+Z_4+Z_2Z_4g_m} \tag{64}$$

$$z_{21} = \frac{Z_2Z_4(1-g_mZ_3)}{Z_2+Z_3+Z_4+Z_2Z_4g_m} \tag{65}$$

$$z_{22} = \frac{Z_4(Z_2+Z_3)}{Z_2+Z_3+Z_4+Z_2Z_4g_m} \tag{66}$$

If the upper frequency is now limited to that below which all reactive effects can be ignored and assuming that $r_{b'c} \gg r_{bb'}, r_{b'e}, r_{ce}$ (ref 9) the equivalent circuit will reduce to that in figure 4c and the terminal parameters, in terms of the equivalent circuit parameters, become

$$z_{11} = r_{bb'} + r_{b'e} \tag{67}$$

$$z_{12} = 0 \tag{68}$$

$$z_{21} = -r_{b'e}\, r_{ce}\, g_m \tag{69}$$

$$z_{22} = r_{ce} \tag{70}$$

Substituting the above terminal parameter equivalents into equation (49), the overall voltage-gain is

$$A_v = \frac{Z_r - r_{b'e}r_{ce}g_m + Y_f\left[r_{ce}(r_{bb'}+r_{b'e}) + Z_r(r_{bb'}+r_{b'e}+r_{ce}+r_{b'e}r_{ce}g_m)\right]}{k+(r_{bb'}+r_{b'e})\,(k_1r_{ce}+k_3) + k_4r_{ce}+k_2\,(r_{bb'}+r_{b'e}+r_{ce}+r_{b'e}r_{ce}g_m)} \tag{71}$$

Although the gain equation is now expressed as a function of all the circuit and hybrid parameters

$$A_v = f_1 (r_{bb'}, r_{b'e}, r_{ce}, g_m, Z_a, Z_f, Z_g, Z_r, Z_L) \tag{72}$$

it can be assumed that

$$\frac{d}{dT} (Z_a, Z_f, Z_g, Z_r, Z_L) = 0 \tag{73}$$

Hence, the voltage-gain variations due to temperature are determined by the temperature dependence of the parameters $r_{bb'}$, $r_{b'e}$, r_{ce}, and g_m and expressed as

$$\frac{dA_v}{dT} = \frac{\partial A_v}{\partial r_{bb'}} \frac{dr_{bb'}}{dT} + \frac{\partial A_v}{\partial r_{b'e}} \frac{dr_{b'e}}{dT} + \frac{\partial A_v}{\partial r_{ce}} \frac{dr_{ce}}{dT} \frac{\partial A_v}{\partial g_m} \frac{dg_m}{dT} \tag{74}$$

If the temperature coefficient, the change in parameter per degree centigrade, is defined as

$$\theta_i = \frac{d}{dT} (\ln i) = \frac{1}{i} \frac{di}{dT} \tag{75}$$

or

$$\frac{di}{dT} = i\theta_i \tag{76}$$

then equation (74) can be rewritten

$$\frac{dA_v}{dT} = \frac{\partial A_v}{\partial r_{bb'}} (r_{bb'}\theta_b) + \frac{\partial A_v}{\partial r_{b'e}} (r_{b'e}\theta_e) + \frac{\partial A_v}{\partial r_{ce}} (r_{ce}\theta_c) + \frac{\partial A_v}{\partial g_m} (g_m\theta_m) \tag{77}$$

where

$$\theta_b = \frac{1}{r_{bb'}} \frac{dr_{bb'}}{dT} \tag{78}$$

$$\theta_e = \frac{1}{r_{b'e}} \frac{dr_{b'e}}{dT} \tag{79}$$

$$\theta_c = \frac{1}{r_{ce}} \frac{dr_{ce}}{dT} \tag{80}$$

$$\theta_M = \frac{1}{g_m} \frac{dg_m}{dT} \tag{81}$$

Optimizing for the condition of minimum or zero gain variation with respect to temperature,

$$\frac{dA_v}{dT} = 0 \tag{82}$$

leads to the expression

$$\frac{\partial A_v}{\partial r_{bb'}} (r_{bb'}\theta_b) + \frac{\partial A_v}{\partial r_{b'e}} (r_{b'e}\theta_e) + \frac{\partial A_v}{\partial r_{ce}} (r_{ce}\theta_c) + \frac{\partial A_v}{\partial g_m} (g_m\theta_m) = 0 \tag{83}$$

Performing the indicated operation, the design criteria which must be met for constant voltage gain with temperature (in terms of the network and transistor equivalent circuit parameters) for a generalized common-emitter single-stage amplifier are

$$\begin{aligned} & g_m \Big\{ (\theta_m + \theta_e)(C_1 + C_4 r_{ce}) + r_{bb'}(\theta_e - \theta_b)(C_3 + C_2 r_{ce}) \\ & + \theta_c C_1 g_{b'e} r_{ce} + (r_{bb'} + r_{b'e})(C_2 \theta_M r_{ce} + C_3 \theta_e) \Big\} \\ & + g_{b'e} \Big\{ (C_5 + C_6 r_{ce} + C_7 g_{ce})(\theta_b r_{bb'} + \theta_e r_{b'e}) \\ & + \theta_c (r_{bb'} + r_{b'e})(C_8 + C_9 r_{bb'} + C_9 r_{b'e}) + C_{10} \theta_c \Big\} = 0 \end{aligned} \tag{84}$$

where

$$C_1 = -(1+Z_r Y_L)(Z_g + Z_r + Z_g Z_r Y_a) \tag{85}$$

$$C_2 = -(Y_L + Y_f)(1 + Y_a Z_g + Y_f Z_g) \tag{86}$$

$$C_3 = -(1 + Z_r Y_L)(1 + Y_a Z_g + Y_f Z_g) \tag{87}$$

$$C_4 = -(Y_L + Y_f)(Z_g + Z_r + Z_g Z_r Y_a) \tag{88}$$

$$C_5 = Y_f Z_g (1 + Z_r Y_L) - Z_r (Y_L + Y_f)(1 + Z_g Y_a) \tag{89}$$

$$C_6 = Y_f Z_g (Y_L + Y_f) \tag{90}$$

$$C_7 = -Z_r (1 + Z_g Y_a)(1 + Z_r Y_L) \tag{91}$$

$$C_8 = Z_r (Y_f - Y_L)(1 - Z_g Y_a) + Y_f Z_g (1 - Z_r Y_L) \tag{92}$$

$$C_9 = Y_f (1 + Y_a Z_g + Y_f Z_g) \tag{93}$$

$$C_{10} = -Z_r Y_L (Z_g + Z_r + Z_g Z_r Y_a) \tag{94}$$

The generalized design criteria are now considered for three special cases where various combinations of Z_r, Z_g, Y_a, and Y_f are equal to zero.

2.3 Special Cases

Case I: $(Z_r, Y_a, Y_f = 0)$

$$(1+Y_L r_{ce})\left[Z_g(\theta_M+\theta_e) + r_{bb'}(\theta_e-\theta_b)\right] + Z_g r_{ce} g_{b'e} \theta_c + (r_{bb'} + r_{b'e})(Y_L \theta_M r_{ce} + \theta_e) = 0 \tag{95}$$

Case II: $(Y_a, Y_f = 0)$

$$g_m \left\{ (\theta_M+\theta_e)(C_1' + C_4' r_{ce}) + r_{bb'}(\theta_e-\theta_b)(C_3'+C_2' r_{ce}) + \theta_c g_{b'e} r_{ce} C_1' + (r_{bb'} + r_{b'e})(C_2' \theta_M r_{ce} + C_3' \theta_e) \right\}$$
$$+ g_{b'e} \left\{ (C_5' + C_7' g_{ce})(\theta_b r_{bb'} + \theta_e r_{b'e}) + \theta_c C_5' (r_{bb'} + r_{b'e}) + C_{10}' \right\} = 0 \tag{96}$$

where

$$C_1' = - (1 + Z_r Y_L) (Z_g + Z_r) \tag{97}$$

$$C_2' = - Y_L \tag{98}$$

$$C_3' = - (1 + Z_r Y_L) \tag{99}$$

$$C_4' = - Y_L (Z_g + Z_r) \tag{100}$$

$$C_5' = - Z_r Y_L \tag{101}$$

$$C_7' = -Z_r (1 + Z_r Y_L) \tag{102}$$

$$C_8' = -Z_r Y_L \tag{103}$$

$$C_{10}' = -Z_r Y_L (Z_g + Z_r) \tag{104}$$

Case III: $(Z_r = 0)$

$$g_m \left\{ (\theta_M + \theta_e) (C_1'' + C_4'' r_{ce}) + r_{bb'} (\theta_e - \theta_b) (C_3'' + C_2'' r_{ce}) \right.$$
$$\left. + \theta_c C_1'' g_{b'e} r_{ce} + (r_{bb'} + r_{b'e}) (C_2'' \theta_M r_{ce} + C_3'' \theta_e) \right\}$$
$$+ g_{b'e} \left\{ (C_5'' + C_6'' r_{ce}) (\theta_b r_{bb'} + \theta_e r_{b'e}) \right.$$
$$\left. + \theta_c (r_{bb'} + r_{b'e}) (C_9'' r_{bb'} + C_9'' r_{b'e} + C_8'') \right\} = 0 \tag{105}$$

where

$$C_1'' = -Z_g \tag{106}$$

$$C_2'' = - (Y_L + Y_f) (1 + Z_g Y_a + Z_g Y_f) \tag{107}$$

$$C_3'' = -(1 + Z_g Y_a + Z_g Y_f) \tag{108}$$

$$C_4'' = - Z_g(Y_L + Y_f) \tag{109}$$

$$C_5'' = Y_f Z_g \tag{110}$$

$$C_6'' = Y_f Z_g (Y_L + Y_f) \tag{111}$$

$$C_8'' = Y_f Z_g \tag{112}$$

$$C_9'' = Y_f(1 + Z_g + Y_a + Z_g Y_f) \tag{113}$$

By utilizing the temperature coefficients

$$\theta_b = 2.3/T \tag{114}$$

$$\theta_e = 3.2/T \tag{115}$$

$$\theta_M = -1/T \tag{116}$$

$$\theta_c = -0.5/T \tag{117}$$

which Eschelman has shown (ref 1) closely approximates the measured temperature variation of the equivalent circuit parameters for an alloy-junction-type transistor, along with the assumption that $r_{ce} > Z_L > r_{b'e} > r_{bb'}$ and $\theta_c \approx 0$, the special case design criteria are further reduced to:

Case I:

$$Z_g = \frac{r_{b'e}}{2.2} \tag{118}$$

Case II:

$$Z_g = \frac{r_{b'e}}{2.2} - Z_r \tag{119}$$

Case III:

$$Z_g = \frac{r_{b'e}}{2.2+3.2\ \frac{g_{b'e}}{g_m} Y_f - r_{b'e}(Y_a + Y_f)} \tag{120}$$

3. EXPERIMENTAL VERIFICATION

To establish the validity of the developed design criteria, an experiment was performed to determine the voltage-gain stability over wide temperature ranges for various degrees of mismatch relative to the design criteria.

3.1 Method

Employing the monitoring techniques and environmental controls as indicated in figure 5, the voltage gain was measured for the transistorized amplifier circuit shown in figure 6 (special case III), from $-50^{\circ}C$ to $90^{\circ}C$ and at frequencies of 10, 100, and 500 kc. Prior to any measurement of the voltage gain, a minimum of 30 min was allowed for temperature stabilization of the transistor junction once the desired environmental temperature had been reached.

To ascertain the effect of mismatch, Z_g was varied to discrete values of 200, 1000, and 488 ohms, the latter being determined from the design criteria equation (120) for the 2N384-type transistor as the test specimen (Appendix A).

To check independence of load, Z_L values of 2000 and 5000 ohms were used with a Z_g of 488 ohms.

3.2 Results

Figure 7 illustrates the average voltage-gain variations measured for ten 2N384 transistors as a function of temperature at a signal frequency of 100 kc for various values of Z_g and Z_L. The results obtained for the signal frequencies of 10 and 500 kc were almost identical with those in figure 7. The small differences could be attributed to experimental error in measurement, thereby validating the assumption made earlier that reactive effects could be neglected over the frequency band of 10 to 500 kc for this transistor.

It should be noted that the gain variations, shown in figure 7, have been normalized and hence are independent of system gain. The average voltage gain for each Z_g and Z_L combination, of the ten 2N384's measured, is shown in Figure 8.

3.3 Discussion

The apparent discrepancy that optimum stabilization was achieved with a Z_g value of 200 ohms instead of the calculated value of 488 ohms (fig. 7) possibly resulted from using the manufacturer's data-sheet values of $r_{bb'}$, $r_{b'e}$, and g_m instead of values actually measured

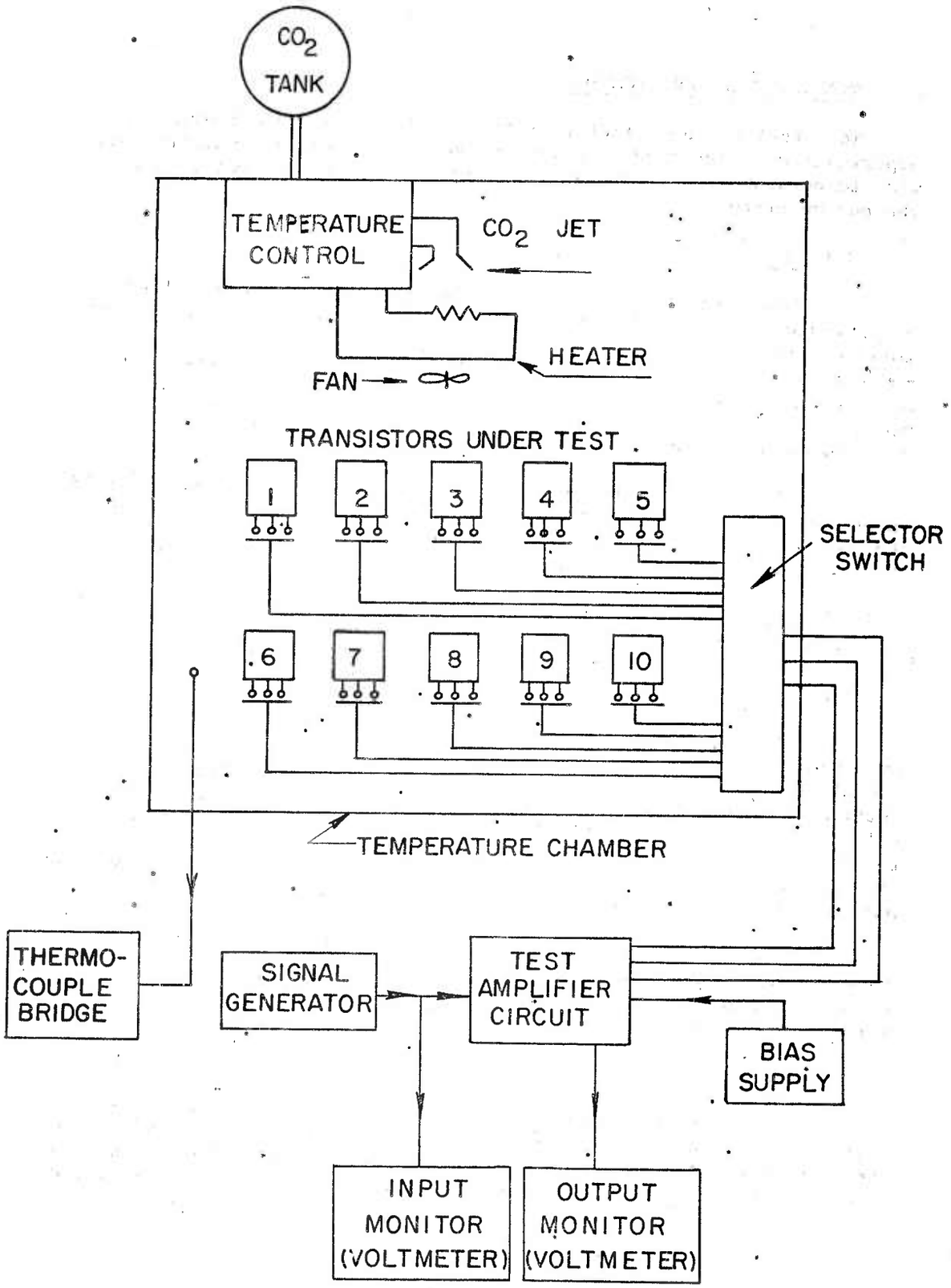


Figure 5. Environmental and monitoring systems.

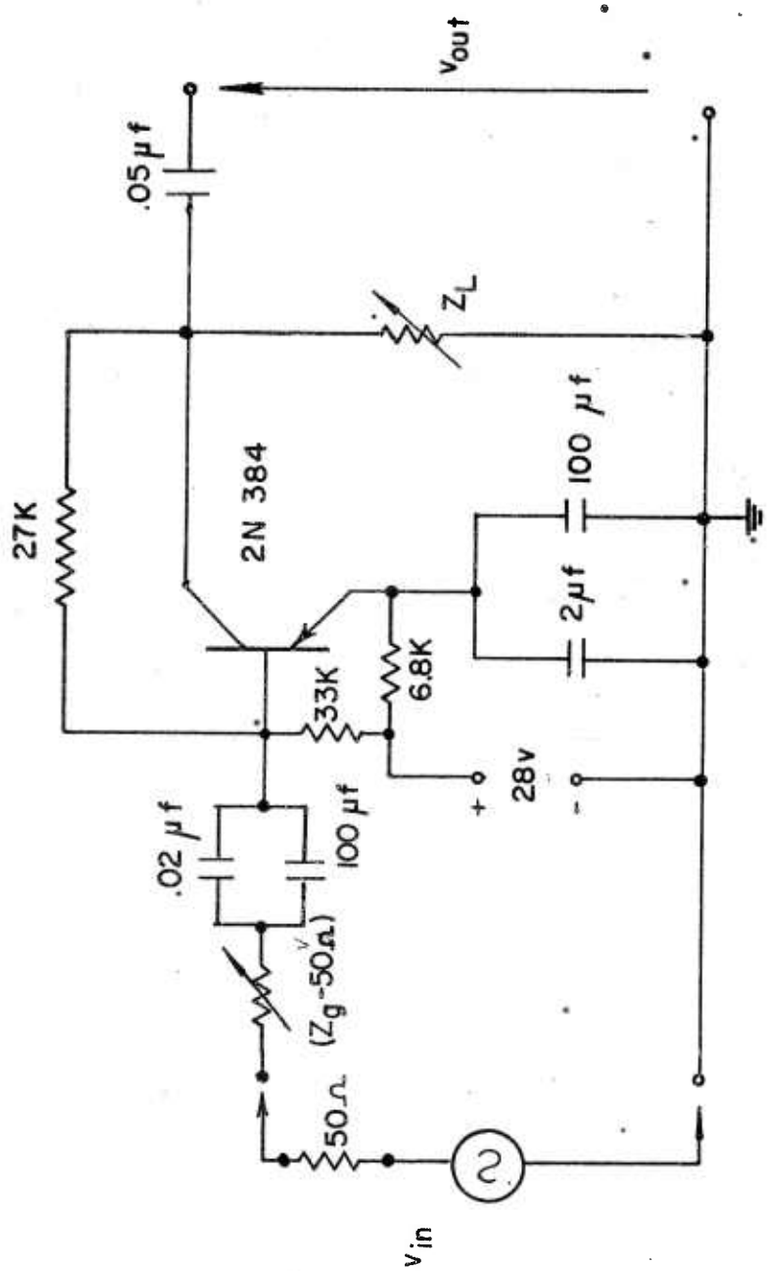


Figure 6. Amplifier circuit used in gain stabilization study.

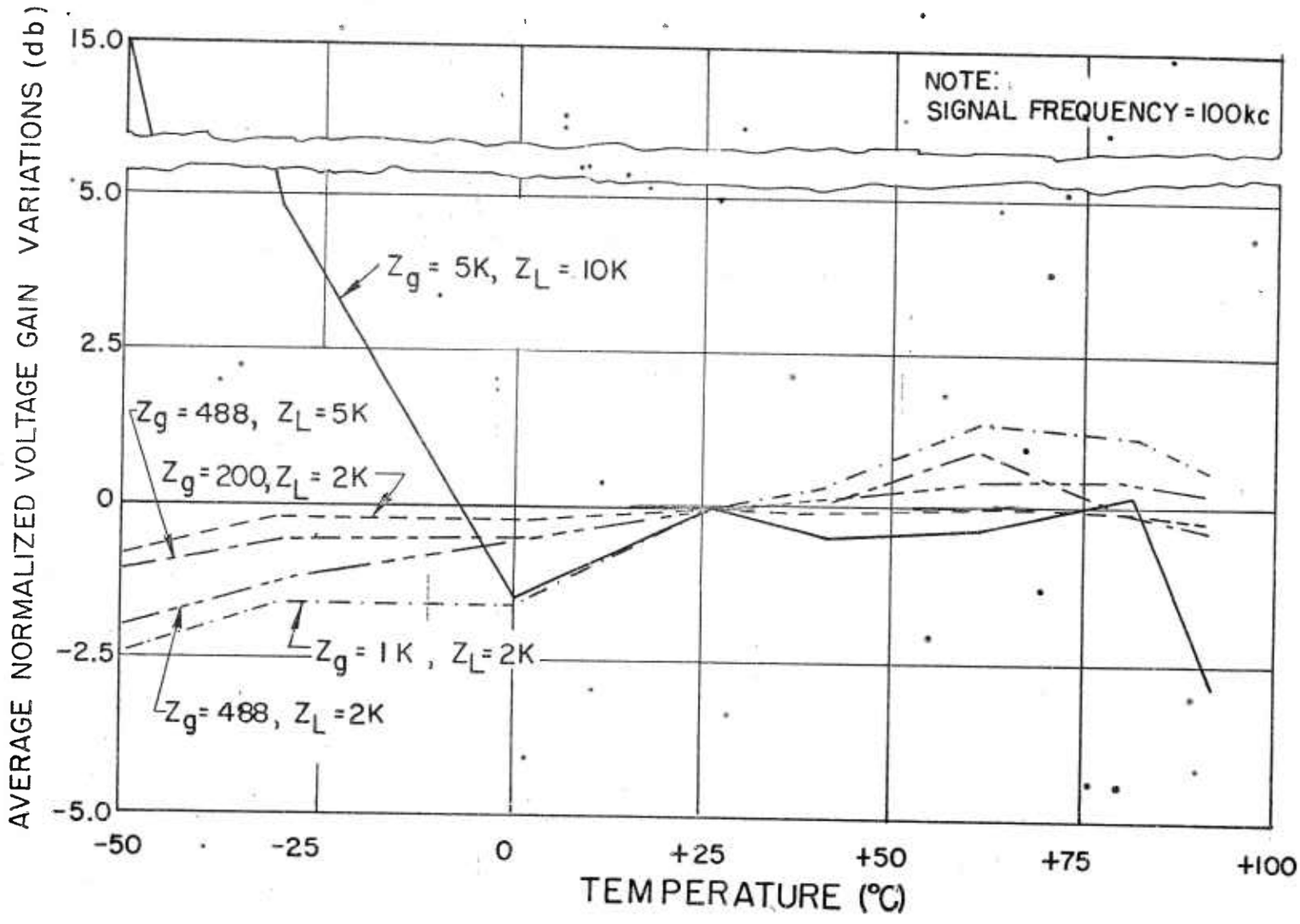


Figure 7. Averaged normalized voltage gain variations versus temperature.

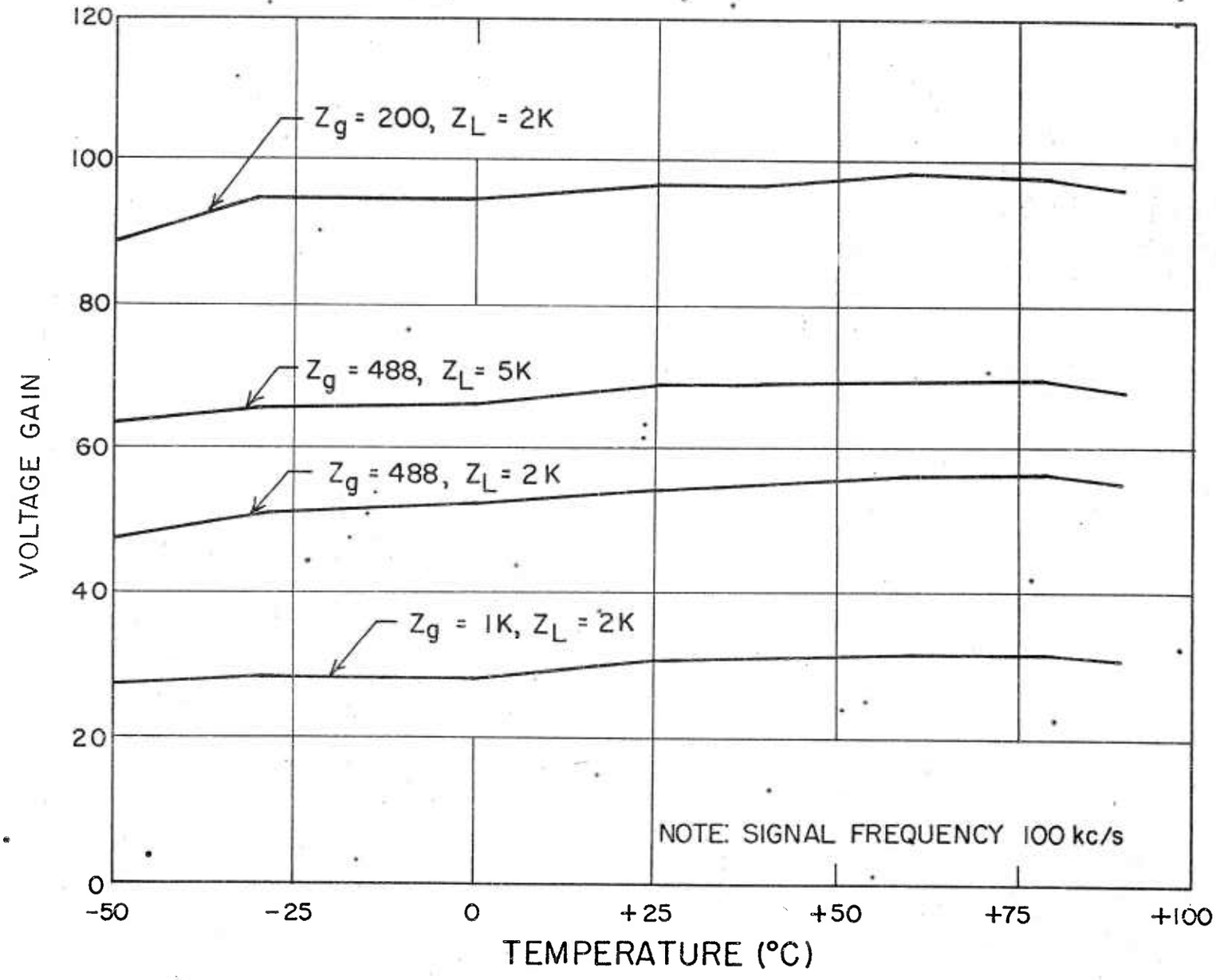


Figure 8. Actual voltage gain versus temperature.

for each transistor, coupled with temperature coefficients not specifically evaluated for this transistor type. This could also explain the slight effect of load (Z_L) on the gain variation, since the load was varied with respect to a Z_g of 488 ohms, which would not have been the matched condition had accurately measured parameters and temperature coefficients for the 2N384 been used.

From the experimental results, it is clearly evident that considerable improvement in the stabilization of gain as a function of temperature can be obtained as the magnitude of Z_g approaches the value specified by the design criteria. However, for this improvement in gain stability some reduction in the overall gain of the system may result. The amount of gain reduction will be dependent upon the ratio of Z_g to the input impedance of the transistor (Z_{11}) as seen in figure 8. Generally, the smaller Z_g is with respect to Z_{11}, the higher the overall gain will be for a given input signal. This will necessitate a compromise value for Z_g in a multistage system, since Z_g will influence the effective load of the preceding stage.

4. CONCLUSIONS

Considerable improvement in gain stability over wide temperature ranges can be obtained with the utilization of the design relationship developed in this investigation. The degree of optimization depends upon the accuracy with which the parameters and temperature coefficients for a particular transistor have been determined, the simplifying approximations, and the amount of gain loss allowed.

5. ACKNOWLEDGMENT

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APPENDIX A

Calculation of Z_g for special case III

Transistor Type - 2N384

Transistor parameter

$$r_{bb'} \approx 50 \text{ ohms}$$

$$r_{b'e} \approx 1040 \text{ ohms}$$

$$g_m \approx 50 \times 10^{-3} \text{ mhos}$$

$$f_\alpha \approx 100 \text{ mc/s}$$

Circuit parameters

$$Z_f = 27 \times 10^3 \text{ ohms}$$

$$Z_a = 33 \times 10^3 \text{ ohms}$$

$$Z_g = \frac{r_{b'e}}{2.2 + 3.2 \frac{Y_f \, g_{b'e}}{g_m} - r_{be} \, (Y_a + Y_f)} \qquad (120)$$

$$Z_g = 488 \text{ ohms}$$

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The normalized gain variations were reduced from a maximum of 18 db to less than 2 db over the temperature range.

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